What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of forming a semiconductor device, comprising the steps of:

forming at least one empty-spaced pattern beneath a surface of, and within a, semiconductor substrate, said empty-spaced pattern being surrounded by semiconductor material;

forming at least one opening within said semiconductor substrate, said opening connecting a respective empty-spaced pattern with the exterior of said semiconductor substrate; and

forming a conductive material in said empty-spaced pattern and said opening.

2. The method of claim 1, wherein the act of forming said empty-spaced pattern further comprises the act of forming at least one hole within said semiconductor substrate and heat treating said substrate to form said empty-spaced pattern beneath said surface of said semiconductor material.

3. The method of claim 2, wherein said hole is a cylindrical hole.

4. The method of claim 2, wherein said semiconductor substrate is heat treated at a temperature of about 1100°C.

5. The method of claim 4, wherein said semiconductor substrate is heat treated under a hydrogen ambient.

6. The method of claim 4, wherein said semiconductor substrate is heat treated for about 60 seconds.

7. The method of claim 1, wherein said empty-spaced pattern has a pipe-shaped configuration.

8. The method of claim 1, wherein said empty-spaced pattern has a spherical configuration.

9. The method of claim 1, wherein said empty-spaced pattern has a plate-shaped configuration.

10. The method of claim 1, wherein said at least one empty-spaced pattern comprises at least one pipe-shaped pattern and at least one plate-shape pattern.

11. The method of claim 10, wherein said at least one pipe-shaped pattern and said at least one plate-shape pattern are formed simultaneously.

12. The method of claim 10, wherein said at least one pipe-shaped pattern and said at least one plate-shape pattern are formed sequentially and before said act of forming said conductive material.

13. The method of claim 1 further comprising the act of forming a barrier layer in said opening and said empty-spaced pattern before said act of forming said conductive material.

14. The method of claim 13 further comprising the act of oxidizing said opening and said empty-spaced pattern before said act of forming said barrier layer.

15. The method of claim 1 further comprising the act of oxidizing said opening and said empty-spaced pattern before said act of forming said conductive material.

16. The method of claim 1, wherein said act of forming said conductive material further comprises depositing a conductive material inside said opening and said empty-spaced pattern.

17. The method of claim 16, wherein said conductive material is formed of a material selected from the group consisting of copper, copper alloy, silver, silver alloy, gold, gold alloy, tungsten, tungsten alloy, aluminum, and aluminum alloy.

18. The method of claim 16 further comprising the step of chemical mechanical polishing said substrate to remove said conductive material on a surface thereof.

19. The method of claim 1, wherein said semiconductor substrate is a silicon substrate.

20. The method of claim 1, wherein said semiconductor substrate is a germanium substrate.

21. The method of claim 1, wherein said semiconductor substrate is a silicon-on-insulator substrate.

22. The method of claim 1, wherein said semiconductor substrate is a silicon-on-nothing substrate.

23. A method of forming at least one buried conductor pattern in a monocrystalline substrate, said method comprising the steps of:

forming a plurality of cylindrical holes in said monocrystalline substrate;

annealing said monocrystaline substrate to form at least one empty-spaced pattern within, and surrounded by, said monocrystalline substrate and below a surface of said monocrystalline substrate;

forming at least one opening in said monocrystaline substrate which communicates with a respective empty-spaced pattern; and

forming a conductive material in said empty-spaced pattern.

24. The method of claim 23, wherein said act of annealing is performed under a reducing atmosphere.

25. The method of claim 24, wherein said reducing atmosphere is a hydrogen atmosphere at a temperature lower than the melting temperature of said monocrystalline substrate.

26. The method of claim 25, wherein said act of annealing is performed for about 60 seconds.

27. The method of claim 23, wherein said empty-space pattern is a pipe-shaped pattern.

28. The method of claim 23, wherein said empty-space pattern is a plate-shaped pattern.

29. The method of claim 23, wherein said empty-space pattern is a sphere-shaped pattern.

30. The method of claim 23, further comprising the act of forming at least two empty-spaced patterns.

31. The method of claim 30, wherein said at least two empty-spaced patterns are simultaneously formed.

32. The method of claim 30, wherein one of said empty-spaced patterns is located below said other empty-spaced pattern relative to said surface of said monocrystalline substrate.

33. The method of claim 23 further comprising the act of forming a barrier layer in said opening and said empty-spaced pattern before said act of forming said conductive material.

34. The method of claim 33 further comprising the act of oxidizing said opening and said empty-spaced pattern before said act of forming said barrier layer.

35. The method of claim 23 further comprising the act of oxidizing said opening and said empty-spaced pattern before said act of forming said conductive material.

36. The method of claim 23, wherein said act of forming said conductive material further comprises depositing a conductive material inside said empty-spaced pattern through said opening.

37. The method of claim 36, wherein said conductive material is formed of a material selected from the group consisting of copper, copper alloy, silver, silver alloy, gold, gold alloy, tungsten, tungsten alloy, aluminum, and aluminum alloy.

38. The method of claim 36 further comprising the step of chemical mechanical polishing said substrate to remove said conductive material on a surface thereof.

39. The method of claim 23, wherein said act of forming said conductive material further comprises forming said conductive material in said opening.

40. The method of claim 23 further comprising the act of forming a second conductive material in said opening, said second conductive material being different than said conductive material in said empty-spaced pattern.

41. The method of claim 40, wherein second conductive material is formed of a material selected from the group consisting of copper, copper alloy, silver, silver alloy, gold, gold alloy, tungsten, tungsten alloy, aluminum, and aluminum alloy.

42. The method of claim 23, wherein said monocrystalline substrate is a silicon substrate.

43. The method of claim 23, wherein said monocrystalline substrate is a germanium substrate.

44. The method of claim 23, wherein said monocrystalline substrate is a silicon-on-insulator substrate.

45. The method of claim 23, wherein said monocrystalline substrate is a silicon-on-nothing substrate.

46. An integrated circuit substrate comprising at least one buried conductor pattern provided within a monocrystalline substrate and surrounded by semiconductor material, and a conductive path extending from said buried conductor pattern.

47. The integrated circuit of claim 46, wherein said buried conductor pattern has a pipe-shaped pattern.

48. The integrated circuit of claim 46, wherein said buried conductor pattern has a plate-shaped pattern.

49. The integrated circuit of claim 46, wherein said buried conductor pattern has a spherical pattern.

50. The integrated circuit of claim 46, wherein said buried conductor pattern comprises a conductive material.

51. The integrated circuit of claim 50, wherein said conductive material is selected from the group consisting of copper, copper alloy, silver, silver alloy, gold, gold alloy, tungsten, tungsten alloy, aluminum and aluminum alloy.

52. The integrated circuit of claim 46, wherein said monocrystalline substrate is a silicon substrate.

53. The integrated circuit of claim 46, wherein said monocrystalline substrate is a germanium substrate.

54. The integrated circuit of claim 46, wherein said monocrystalline substrate is a silicon-on-insulator substrate.

55. The integrated circuit of claim 46, wherein said monocrystalline substrate is a silicon-on-nothing substrate.

56. A buried conductor pattern within a substrate, comprising:

at least one empty-spaced pattern in said substrate formed by annealing said substrate containing at least one hole drilled therein; and

a conductive material filling said empty space pattern.

57. The buried conductor pattern of claim 56 further comprising a conductive via connecting said conductive material with a surface of said substrate.

58. The buried conductor pattern of claim 56, wherein said empty-spaced pattern has a pipe-shaped configuration.

59. The buried conductor pattern of claim 56, wherein said empty-spaced pattern has a plate-shaped configuration.

60. The buried conductor pattern of claim 56, wherein said empty-spaced pattern has a sphere-shaped configuration.

61. The buried conductor pattern of claim 56, wherein said substrate is a monocrystalline substrate.

62. A processor system comprising:

a processor; and

a circuit coupled to said processor, at least one of said circuit and processor comprising:

a conductive structure comprising a substrate having at least one empty space pattern formed by annealing said substrate having at least one hole drilled therein; and

a conductive material filling said empty space pattern.

63. The processor-based system of claim 62, wherein said empty-spaced pattern has a configuration selected from the group consisting of pipe-shaped configuration, sphere-shaped configuration and plate-shaped configuration.

64. The processor system of claim 62, wherein said empty-spaced pattern has a plate-shaped configuration.

65. The processor system of claim 62, wherein said empty-spaced pattern has a sphere-shaped configuration.

66. The processor system of claim 62, wherein said substrate is a monocrystalline substrate.

67. The processor system of claim 62, wherein said circuit is a memory circuit.

68. The processor system of claim 62, wherein said circuit is a DRAM memory circuit.

69. The processor system of claim 62, wherein said circuit and said processor are integrated on same circuit.

70. The processor system of claim 62, wherein said processor comprises said conductive structure.

71. The processor system of claim 62, wherein said circuit comprises said conductive structure.

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